REMARKS

Claims 1-4 and 7-12 are pending in this application. Claims 1-4 and 7 were examined on the merits in the last Office Action. Claims 8-12 remain withdrawn from consideration. With the present submission, claim 1 is amended.

Claims 1-4 and 7 stand rejected under 35 U.S.C. § 103(a) as obvious over the prior art depicted in the present application, labeled "Admitted Prior Art (**APA**)," in view of **Cook et al.** (U.S. Patent No. 6,022,791) and **Chiang et al.** (U.S. Patent No. 5,817,572). Applicant respectfully submits that the rejection should be withdrawn.

Base claim 1, as currently amended, describes a semiconductor device such that:

> said conductive pattern and said second insulation film [have] coplanar top principal surfaces,
>
> a bottom edge of said conductive wall [makes] an intimate contact with said top principal surface of said conductive pattern, and
>
> said conductive pattern and said second insulation film located at a top part of said multilayer interconnection structure [are] covered continuously with an insulation film.

Applicant submits that the applied prior art does not suggest these features.

For example, applicant references first the Office Action, page 4, top, which shows that the rejection relies on the **Chiang et al.** etch-stop layer 323 (shown in Fig. 25) as teaching a "second insulation film." Applicant now refers to Fig. 7 of the present application, which shows that the "conductive pattern" and the "second insulation film" of the present invention have a coplanar top principal surfaces. This feature is now explicitly recited in base claim 1, as shown above, and the

device of **Chiang et al.**'s Fig. 25 does not have this feature. Accordingly, the obviousness rejection should be withdrawn for at least this reason alone.

Nonetheless, claim 1 distinguishes applicant's invention from the applied prior art in at least another way: Note that the guard ring of **Cook et al.** is exposed to the environment at the top of the multilayer interconnection structure. In contrast, applicant's invention has a protective insulation film at the top of the multilayer interconnection structure. (Note, for example, applicant's Fig. 7, which shows protective film 46 formed of SiN, as discussed in the specification, page 14, lines 26-28.) The feature of the conductive pattern and the second insulation film located at a top part of said multilayer interconnection structure being covered continuously with an insulation film is now explicitly recited in base claim 1. Accordingly, the obviousness rejection should be withdrawn this additional reason.

Claims 2-4 and 7 depend from claim 1, so the obviousness rejection of those claims should also be withdrawn for at least the reason of their dependencies.

In view of the amendments and remarks above, applicant further submits that the entire application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is felt that this application is not now in condition for allowance, the Examiner is invited to contact applicant's undersigned attorney at the telephone number indicated below to arrange for disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version of Amendments with Markings to Show Changes Made**."

In the event that this paper is not timely filed, applicant petitions for an appropriate extension of time. The fees for such an extension, or any other fees which may be due, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,
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Enclosure: Version of Amendments with Markings to Show Changes Made

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VERSION OF AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS:

1. (Five Times Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate when viewed in a direction perpendicular to said principal surface of said substrate,

and wherein said interlayer insulation films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally,

said conductive wall and conductive pattern comprising Cu.

said conductive pattern and said second insulation film having coplanar top principal surfaces,

a bottom edge of said conductive wall making an intimate contact with said top principal surface of said conductive pattern, and

said conductive pattern and said second insulation film located at a top part of said multilayer interconnection structure being covered continuously with an insulation film.